LOW-POWER MODE CLOCK MANAGEMENT FOR WIRELESS COMMUNICATION DEVICES

Bruce E. Edwards

Mark D. Matson

ABSTRACT OF THE DISCLOSURE

[039] A power management scheme for a wireless communications device substantially implemented on a single CMOS integrated circuit is described. The present invention provides a method and apparatus for generating first and second clock signals for a wireless communication device, with the first and second clock signals corresponding first and second power levels, depending on the operating mode of the wireless communication unit. In the first operating state, the transceiver in the RF analog module is operational and the clock generator provides a first clock signal having the high-speed, high-accuracy characteristics necessary to maintain efficient operation of the transceiver. In a second operating state, the transceiver in the RF analog module is turned off. In this second operational state, the clock generator provides a second clock signal having a frequency and quality sufficient to maintain efficient operation of the digital modules in the wireless communication device. In the second operational state, the high-speed, high-accuracy clock is replaced by a low-power oscillator when the wireless communication unit is operating in a low power mode.